METHODOLOGY FOR CREATING EMBEDDED TRANSMISSION LINE 90° BEND AND SHUNT CAPACITOR MODELS

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Abstract—This paper describes a technique for creating embedded transmission line (ETL) 90° bend and high current handling shunt capacitor models for monolithic microwave integrated circuits (MMIC). This procedure is generally applicable and may be used to develop working scaleable models for new MMIC topologies. Using the method outlined below, a unique design library may be easily constructed to offer a more complete and accurate modeling capability than may be presently available with commercial microwave CAD tools.

I. INTRODUCTION

A cross section of an embedded transmission line (ETL) field effect transistor (FET), shunt capacitor, and inverted microstrip line is shown in Figure 1. The circuit structures are placed between the gallium arsenide (GaAs) and a 25μm thick layer of polyimide covered with a solid gold ground plane. Gold vias extend through the polyimide up to the ground plane. ETL MMICs were first described in [1] and a flip-chip 1 watt amplifier package was described in [2] and demonstrates the advantages and usefulness of this new topology.

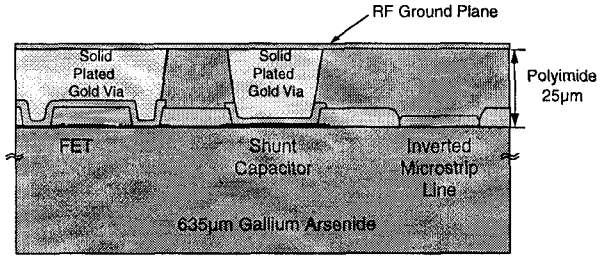

Fig 1. ETL MMIC structure for a FET, shunt capacitor and inverted microstrip transmission line.

The ETL topology is a new type of transmission line for the design of flip-chip MMICs. The embedded transmission line resembles an inverted microstrip line, however, a polyimide gap instead of an air gap is used between the transmission line and the ground plane. The effective dielectric constant (ε_{eff}) for embedded transmission lines decreases with the increasing line width in contrast to microstrip lines where ε_{eff} increases with the increasing line width. For this reason, microstrip models are invalid for embedded transmission line models. New procedures must be developed to create new models that accurately predict the performance of various ETL circuit structures. This paper presents an empirical approach that is rapidly applied to two example ETL structures: a 90° bend and a shunt capacitor.

II. MODELING APPROACH

To begin the modeling process, several layout files are created and electromagnetic simulations are performed using Sonnet's *em*™. The generated S-parameter files are imported into Libra Series IV™ where a circuit model is optimized to fit the simulated data. Once the optimized parameter values are obtained for each file, the circuit model parameters are plotted versus the varied parameter. Next, carefully chosen empirical functions of the varied parameter are fit to each circuit element model. These empirical equations with the fitted coefficients are then inserted into a Libra schematic element to produce scaleable models for use in MMIC designs.

III. ETL MODEL EXAMPLES

Case A. ETL 90° bend

Figure 2 shows an ETL bend created using *xgeom*™. The embedded transmission line metal thickness (5μm) must be modeled for accurate simulation results because it is a significant fraction of the polyimide thickness (25μm). Ports 1 and 2 exist on both layers and are tied together electrically through

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software and each port is de-embedded to the edge of the bend.

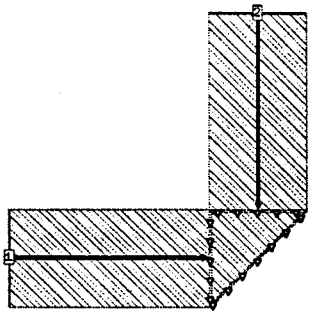

Fig. 2. An ETL 90° bend Sonnet *xgeom* plot of one metal layer.

Table I shows the dielectric layers and metallization levels of the ETL 90° bend model. The metal patterns are found on levels 0 and 1 with a 5μm thick polyimide dielectric located between these two metal levels. The bend is simulated in Sonnet's *em* software with transmission line widths of 5 - 200μm over a frequency range of 5 - 50 GHz.

TABLE I
XGEOM ETL BEND DIELECTRIC PARAMETERS

Level	Thickness uM	Erel	Loss Tan	Bulk Cond S/m
Top				
0 ---	[illegible]	[illegible]	[illegible]	[illegible]
1 ---	5.00000	4.00000	0.00200	0.00000
	20.0000	4.00000	0.00200	0.00000

The circuit model used for the 90° bend is shown in Figure 3. It is a symmetrical *T*-network with parameters *C*, *R*, and *L* which are optimized to fit the simulated Sonnet S-parameters for each line width.

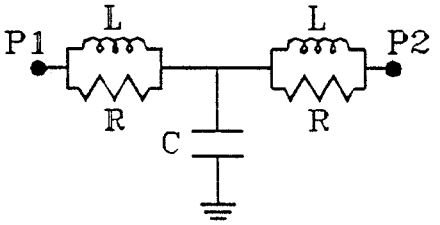

Fig. 3. Libra circuit model for the ETL 90° bend.

Figure 4 displays the modeled *C*, *R*, and *L* values versus bend width in microns. KaleidaGraph™ software is used to create the smooth curve fits for each element using empirically chosen curve fitting equations (1)-(3). The width *w*(μm) is the parameter that is entered in the Libra schematic element by a user. In this example, the ETL transmission line bend model is valid from 5μm - 200μm.

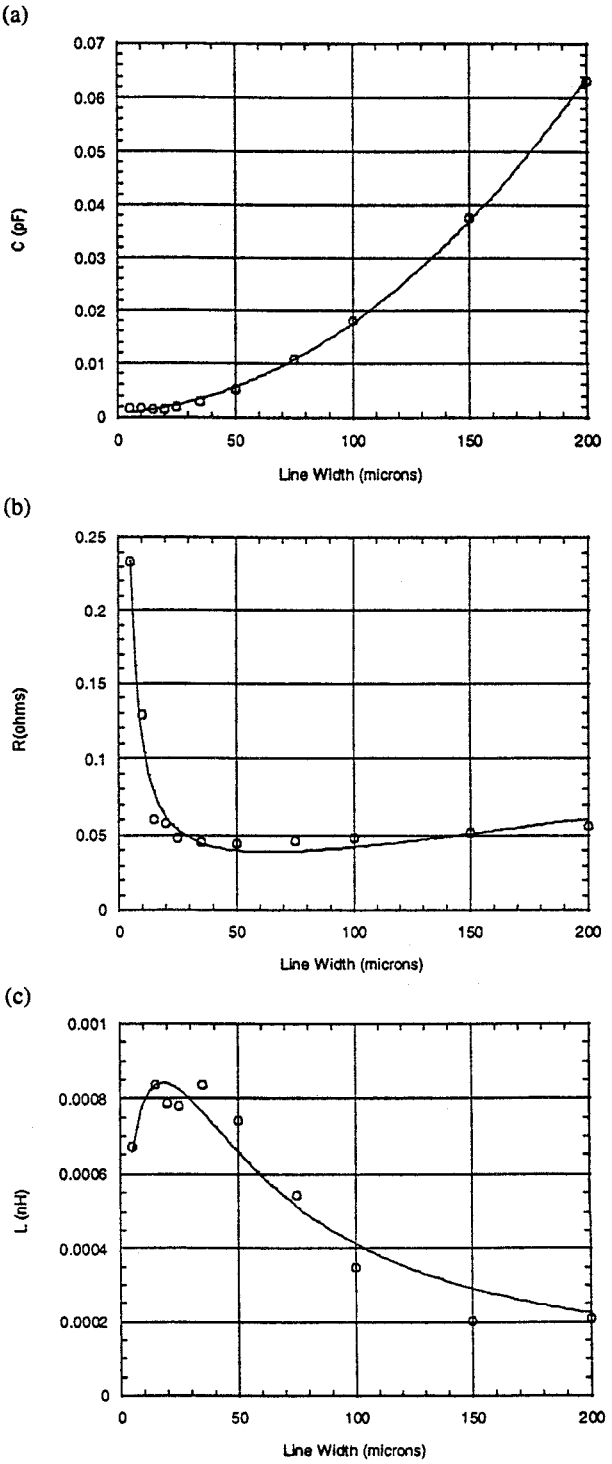

Fig. 4. Modeled a) capacitance, b) resistance, and c) inductance versus line width for the ETL 90° bend with included curve fit.

$$C(pF) = 8.256e-04 + 2.365e-05w + 1.450e-06w^2 \quad (1)$$

$$R(\Omega)=\frac{0.91415}{w-0.91415}+0.000234(w+149)-0.0252 \quad (2)$$

$$L(nH)=0.048048\left(1-e^{-\frac{w}{24.215}^{0.11}}\right)\Big/w+14.741 \quad (3)$$

Case B. ETL shunt capacitor

The ETL shunt capacitor *xgeom* model includes four layers of metallization with each layer connected to the next through a network of vias. The top layer is a completely metallized gold ground plane that is plated on top of the polyimide dielectric. The next layer shown in figure 5a is the plating/bridge layer. The plating models the 5μm metal thickness between it and the capacitor top plate. Figure 5b shows the next metal layer which is made up of the capacitor top plate and the thin via strips on either side that provide connection to the bridges. The final metal layer includes two ports, feed lines, and via strips that provide a connection to the bridges (figure 5c). The two circular shunt vias at the top and bottom are connected from each layer to ground.

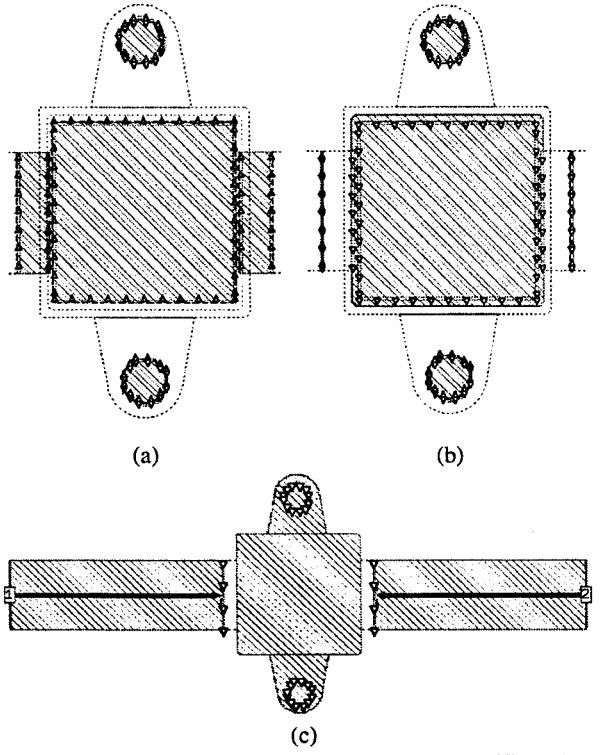

Fig. 5. Sonnet Software's *xgeom* layout of the ETL shunt capacitor (gold ground plane layer not shown). a) Plating / bridge layer. b) Top plate layer. c) First metal layer.

Figure 6 shows a cross-section of this ETL MMIC shunt capacitor. At the top of the photo is an air layer followed by the gold ground plane. Between the ground plane and the GaAs (at the bottom) is a 25μm thick polyimide dielectric layer. The transmission line is shown in the center and is located between the polyimide and the GaAs substrate.

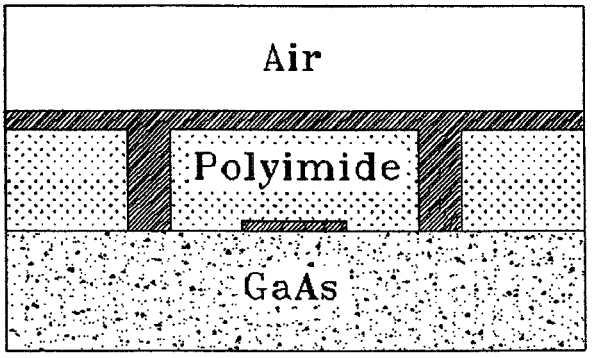

Fig. 6. Cross-section of an ETL MMIC side grounded shunt capacitor.

The shunt capacitor has been simulated at values ranging from .3pF - 20pF over a frequency range of 5 - 50 GHz.

The circuit model used for the shunt capacitor is shown in Figure 7. To eliminate variables and simplify the design process, R1, R2, and L were set to carefully chosen constants. Parameters l_1 and l_2 are the line lengths of TLIN1 and TLIN2, respectively, and C_{half} is equal to $C_{total}/2$. Two different line widths (25μm, 80μm) were chosen for TLIN1 for certain ranges of C_{total} due to design constraints.

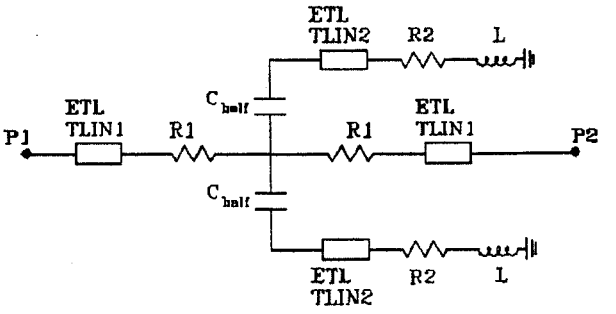

Fig. 7. Libra circuit model for the ETL shunt capacitor.

Figure 8 shows the plotted values of C_{half} and l_1-l_2 for each particular range along with the fitted function. These values were obtained after the circuit model was optimized to the electromagnetic simulated response. When the TLIN1 width is equal to 25μm, range 1 should be used and when TLIN1 is equal to 80μm, range 2 should be used. The width of TLIN1 is equal to 25μm for $.3pF \le C_{total} \le 2pF$ and 80μm for $2pF \le C_{total} \le 20pF$.

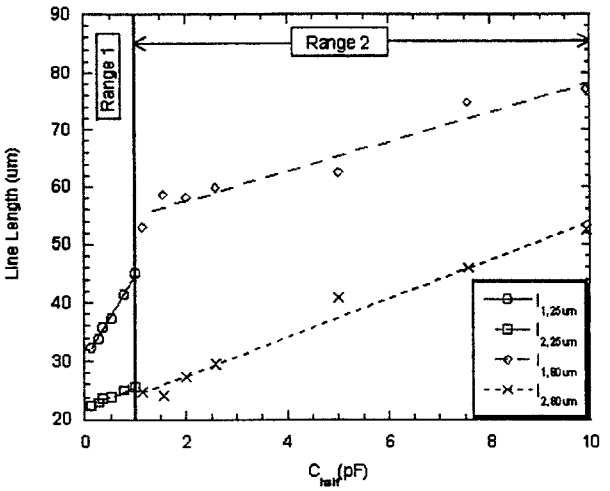

Fig. 8. ETL shunt capacitor line lengths for 25μm (range 1) and 80 μm (range 2) wide TLIN1 versus simulation parameter C_{half}.

Figure 9 shows measured data from a 2.2pF shunt capacitor versus the newly created shunt capacitor Libra scaleable model with C_{total} = 2.2pF. The model demonstrates an excellent fit to the measured data up to 40 GHz.

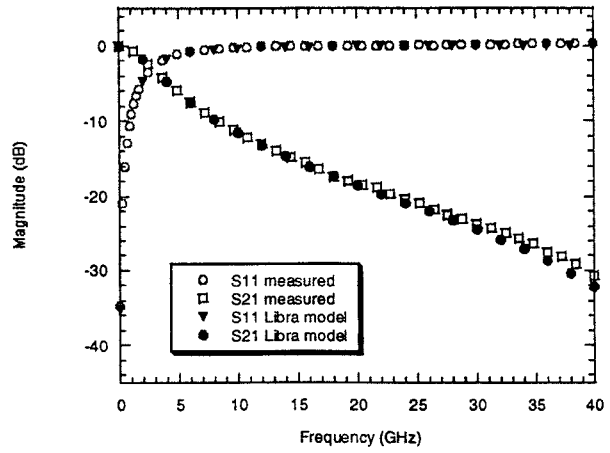

Fig. 9. Measured versus modeled data for a 2.2pF shunt capacitor.

Equations (4)-(12) characterize the model of the shunt capacitor. The KaleidaGraph software curve fits for .3pF ≤ C_{total} ≤ 2pF are listed in equations (8)-(9), and the curve fits for 2pF ≤ C_{total} ≤ 20pF are listed in equations (10)-(11). $W(\mu m)$ is the dimension of the square capacitor top plate which is used to link the model to the physical layout. C_{total} is the parameter that will be entered by the user in Libra, and from this, all other variables can be solved for by using the equations in the Libra scaleable model.

$$R1(\Omega) = 0.1078 \quad (4)$$

$$R2(\Omega) = 0.0386 \quad (5)$$

$$L(nH) = .003686 \quad (6)$$

$$C_{half}(pF) = C_{total}/2 \quad (7)$$

$$l_{1,25\mu m} = 30.063 + 14.969C_{half} \quad (8)$$

$$l_{2,25\mu m} = 22.039 + 3.7336C_{half} \quad (9)$$

$$l_{1,80\mu m} = 52.334 + 2.6025C_{half} \quad (10)$$

$$l_{2,80\mu m} = 20.915 + 3.3094C_{half} \quad (11)$$

$$W(\mu m) = 57.244C_{half}^{.50114} \quad (12)$$

IV. Conclusion

This paper described a unique process of creating scaleable MMIC element models. This process may easily be repeated on other structures to develop application specific scaleable model libraries. Up to this point in time no known models for ETL 90° bends and side grounded shunt capacitors exist. These structures are important for ETL MMIC design. Using the procedure presented and with a few days worth of effort, new models of scaleable elements can be created without the need for discrete electromagnetically simulated S-parameter files to be inserted later in the schematic. This procedure is not only valid on basic ETL elements but also is a targeted solution for new MMIC topologies.

Acknowledgment

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References

1. H. Tserng, , P. Saunier, A. Ketterson, L. Witkowski, T. Jones, "Embedded Transmission Line (ETL) MMIC for Low-Cost, High-Density Wireless Communication Applications," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 41-44, 1997.

2. T. Budka, A. Ketterson, H. Tserng, L. Stiborek, L. Heinrich, R. Smith, B. Ables, C. Kyhl, K. Worthen, G. Brehm and J. Reddick, "Embedded Transmission Line MMIC 1 Watt Flip Chip Assembly Using a Z-Axis Interconnect" To be published in *IEEE Microwave and Guided Wave Letters.*